DB Name	Query	Hit Count	Set Name
USPT	l24 same scan	4	L25
USPT	l22 same l23	66	L24
USPT	self-test	3585	L23
USPT	probe	97652	L22
USPT	l15 same speed	86	L21
USPT	l17 same speed	1	L20
USPT	l17 same scan	16	L19
USPT	l17 same clock	12	L18
USPT	l15 same processor	91	L17
USPT	l13 same l15	11	L16
USPT	bist	610	L15
USPT	l12 same l13	5	L14
USPT	internal near3 clock	10629	L13
USPT	l9 same l10	1036	L12
USPT	l8 same l9	3	L11
USPT	scan	111938	L10
USPT	ic	68692	L9
USPT	service adj1 processor	862	L8
USPT	l1 same core	3	L7
USPT	ip adj3 core	15	L6
USPT	l1 and l3	8	L5
USPT	l1 same l3	1	L4
USPT	embedded adj3 core	1283	L3
USPT	l1 adj3 core	1	L2
USPT	intellectual adj1 property	2633	L1

WEST

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L19: Entry 7 of 16 File: USPT Jun 2, 1998

DOCUMENT-IDENTIFIER: US 5761489 A
TITLE: Method and apparatus for scan testing with extended test vector storage in a multi-purpose memory system

DEPR:
In summary, the above specification describes a method and apparatus for performing BIST scan testing using memory internal to the data processor 12 for storing an extended set of test vectors.

DEPR:
In one embodiment of the present invention illustrated in FIG. 3, all of the circuitry but the AND gate 102, S/R latch 120 and counters 106 and 110 were already being used by CPU 20 for other functions in a normal operating mode which were unrelated to the present invention. In addition, the conventional shift register used to read and write data blocks from and to memory cache 100 was modified to permit it to perform serial to parallel shifting, and address counter 114 was modified to control the directionality of the counter upon assertion of test mode 66. Thus, by adding a relatively small amount of circuitry, CPU 20 was now able to perform BIST scan testing with an extended set of test vectors initially stored in the existing memory internal to the data processor.

WEST

End of Result Set

Generate Collection

L20: Entry 1 of 1 File: USPT Nov 23, 1999

DOCUMENT-IDENTIFIER: US 5991898 A
TITLE: Arithmetic built-in self test of multiple scan-based integrated circuits

BSPR:
In BIST, the original circuit designed to perform the system functions is appended with additional circuitry for generation of test patterns.sup.1 and compaction of test responses. Thus, the BIST approach can be applied at all levels of testing, starting from wafer and device to system and field testing. Appending these circuitry to the original circuit satisfies the high fault coverage requirement while reducing the dependence on expensive external testing equipment. However, this solution compromises an IC's area and performance as it inevitably introduces either a hardware overhead or additional delays and increased latency. These delays may be excessive for high-speed ICs used in several applications such as high-performance microprocessors, digital signal processing (DSP) systems, new generations of floating point processors, and others. Therefore, BIST schemes are often evaluated on the basis of the fault coverage they provide, area overhead they require, and the performance penalty they produce. Other criteria include test application time, scalability, and test-pattern portability. For further description of BIST, see, for example, V. D. Agrawal, C. R. Kime, and K. K. Saluja, "A Tutorial on Built-In Self Test. Part 1: Principles", IEEE Design and Test of Computers, March 1993, pp. 73-82, and V. D. Agrawal, C. R. Kime, and K. K. Saluja, "A Tutorial on Built-In Self-Test. Part 2: Applications", IEEE Design and Test of Computers, June 1993, pp. 69-73.

BSPR:
Circuits based on data-path architectures constitute an increasingly large portion of integrated chips manufactured by the microelectronics industry. The proliferation of embedded cores and high-performance computing systems, such as DSP circuits, micro-controllers, and micro-processors clearly demonstrates inadequacy of existing BIST schemes if they are to entail non-intrusive, at-speed and portable testing. Recently, a new BIST paradigm was proposed by S. Adham, M. Kassab, N. Mukherjee, K. Radecka, J. Rajski, and J. Tyszer in the paper entitled "Arithmetic built-in self-test for digital signal processing architectures", Proc. CICC, pp. 659-662, 1995, which makes it possible to use the functionality of these circuits (also referred to as mission logic or mission data paths) to perform built-in self-test for a DSP core rather than adding test hardware which can introduce area overhead and performance degradation. The resulting test sessions are controlled by microcode and use the mission data path building blocks, such as adders, multipliers, and ALUs, to generate test patterns for a DSP core, and compact its test responses. In such an environment, the need for extra hardware is either entirely eliminated or drastically reduced, test vectors are easily distributed to different parts of the DSP core, test responses are easily collected, and there is virtually no performance degradation. Furthermore, the approach can be used for at-speed testing, thereby providing a capability to detect failures that may not be detected by conventional low-speed testing. However, the ABIST proposal presented in the Adham article did not address generation of test patterns for peripheral devices, in particular, peripheral devices with "shortened" multiple scan-chains in ICs.

WEST

Generate Collection

L19: Entry 3 of 16 File: USPT Nov 23, 1999

DOCUMENT-IDENTIFIER: US 5991898 A
TITLE: Arithmetic built-in self test of multiple scan-based integrated circuits

BSPR:
Circuits based on data-path architectures constitute an increasingly large portion of integrated chips manufactured by the microelectronics industry. The proliferation of embedded cores and high-performance computing systems, such as DSP circuits, micro-controllers, and micro-processors clearly demonstrates inadequacy of existing BIST schemes if they are to entail non-intrusive, at-speed and portable testing. Recently, a new BIST paradigm was proposed by S. Adham, M. Kassab, N. Mukherjee, K. Radecka, J. Rajski, and J. Tyszer in the paper entitled "Arithmetic built-in self-test for digital signal processing architectures", Proc. CICC, pp. 659-662, 1995, which makes it possible to use the functionality of these circuits (also referred to as mission logic or mission data paths) to perform built-in self-test for a DSP core rather than adding test hardware which can introduce area overhead and performance degradation. The resulting test sessions are controlled by microcode and use the mission data path building blocks, such as adders, multipliers, and ALUs, to generate test patterns for a DSP core, and compact its test responses. In such an environment, the need for extra hardware is either entirely eliminated or drastically reduced, test vectors are easily distributed to different parts of the DSP core, test responses are easily collected, and there is virtually no performance degradation. Furthermore, the approach can be used for at-speed testing, thereby providing a capability to detect failures that may not be detected by conventional low-speed testing. However, the ABIST proposal presented in the Adham article did not address generation of test patterns for peripheral devices, in particular, peripheral devices with "shortened" multiple scan-chains in ICs.

L18: Entry 4 of 12 File: USPT Apr 1, 1997

DOCUMENT-IDENTIFIER: US 5617531 A
TITLE: Data Processor having a built-in internal self test controller for testing a plurality of memories internal to the data processor

DEPR:
Generally, the present invention provides a method and apparatus for internally testing a plurality of memories within a data processor. This testing is accomplished by performing a Memory Built-In-Self-Test (BIST) which can be invoked by transitioning a single external pin on the data processor or alternatively by placing a control word within an internal control register of the data processor and supplying only the data processor functional clock signal. The Built-In-Self-Test (BIST) is accomplished by conducting a sequence of events, that is controlled by a minimal amount of circuitry and is fully self-contained within the data processor.

DEPR:
The actual application order of reads, writes, stall cycles (needed because of the pipelined nature of the memory interface), and pattern data was selected to provide the highest level of fault detection for the data processor. When the BIST is completed, the test controller will transition a package pin of the data processor to indicate the test is done (so no clock counting needs to be done by any external device), and the compressed read data from the memories (known as a signature) will be presented one bit at a time (serially) at another package pin on subsequent clock cycles. Furthermore, a single bit may be output for the data processor to indicate a pass/fail status of the recently tested internal memories of the data processor. This pass/fail bit provides a way to quickly determine if the memories internal to the data processor passed or failed.

DEPR:
The whole 32 bit test pattern word is transferred from the bi-directional test bus 31 to the data processor data bus 44 after one data processor clock cycle, and is transferred to a selected memory 32-bit data input register 18 or 21 or 23 on the next rising edge of the clock. These registers are part of the local memory data path from the CPU 15 and are reconfigured by multiplexers to get their data from the data processor data bus when the BIST mode is established. The overall effect of this architecture is to emulate the application of data at the data pins and to pass this data to a selected memory through a two stage pipeline.

DEPR:
The actual application of BIST reads and writes to particular memories, banks, and word locations, and the data pattern written to these locations has been organized and sequenced in such a way as to get the maximum fault detection for the physical placement of the memory cells. This means that the data patterns 0, F, 5, A, 3, and C have been chosen and applied in a particular sequence to memory locations that have also been addressed in a particular sequence to most aggravate and identify common memory faults such as individual memory bits shorted together that are physically next to each other within a word; bits shorted together within a column; random bits shorted to each other; random bits that are stuck at a logic value of 1 or 0; address lines that select memory locations have shorts to other address lines; address lines that are stuck at logic values of 1 or 0; and memory cell data retention since the BIST can be run at the rated data processor clock frequency.

DEPR:
When the whole BIST is completed, a final signature exists in the memory

verification element 27 and the pattern generator 26 indicates internally that it has created its last test pattern. This causes the BIST done pin 32 to transition, which alerts the user of the data processor that the test is complete (without the user having to count clock cycles). On the clock cycle after the BIST done pin 32 transitions, a BIST good pin presents a pass/fail status that is assessed internal to the data processor by conducting a compare between the final signature value and a predetermined designed-in value. On subsequent clock cycles after the pass/fail status pin transitions, the signature itself is presented serially one bit at a time. The signature can also be transferred to an internal status register at any time during the sequence, and this signature can be viewed by serially presenting it to another output pin (this process is referred to as a accessing a partial signature).

DEPR:
The many unique features documented here, such as the ability to invoke the BIST with a single pin and the clock while not requiring any values to be present on any other input signal pins; not loading down or causing any performance degradation to the functional input and output data processor busses; being able to conduct a full manufacturing defect quality type of test with real data; using parts of the functional memory architecture; and controlling and conducting all of this testing with a minimum hardware impact single test controller that uses only 22 flip-flops for pattern generation and 34 flip-flops for memory verification, make this architecture ideal for many test environments. The above may also be implemented at wafer-level testing stages to predetermine faulty integrated circuits before incurring the cost of packaging the faulty circuits.

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L16: Entry 2 of 11 File: USPT Oct 5, 1999

DOCUMENT-IDENTIFIER: US 5961653 A
TITLE: Processor based BIST for an embedded memory

DEPR:
The clock generator 240 is used to provide options in shaping the array clocks. The front end of circuit 240 is responsive to the state of the two clock inputs, TSTN0 and TSTN1 241 and a plurality of scan-only latch (not shown) states to provide a plurality of internal systems clock options. These options are, among others: a scan mode for LSSD testing, BIST initialization, shaping of a clock pulse by programming the duty factor during initialization, switching from single access mode to page mode, etc.

WEST

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L19: Entry 5 of 16 File: USPT Oct 5, 1999

DOCUMENT-IDENTIFIER: US 5961653 A
TITLE: Processor based BIST for an embedded memory

CLPR:
23. The processor based Built-in Self-Test Macro as recited in claim 1, further comprising: a boundary latch pipe comprised of boundary scan latches coupled to inputs and outputs of the BIST macro, said boundary latch pipe improving test coverage when scanning said latches.

WEST

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L25: Entry 2 of 4 File: USPT Aug 10, 1999

DOCUMENT-IDENTIFIER: US 5936876 A
TITLE: Semiconductor integrated circuit core probing for failure analysis

BSPR:
Finally, built-in self-test is useful as it provides 100% fault coverage in a reasonable test time. Moreover, software tools are known for automatically synthesizing BIST circuitry for compiled memories. However, BIST circuitry adds additional complexity and area to the chip, as described in more detail with reference to FIG. 1, below. Moreover, BIST may be adequate to provide a "good/bad" decision at wafer probe time, but again it does not provide detailed analysis of the failure mode. Accordingly, when an ASIC is presented for failure analysis, and embedded RAM is the suspect, the manual probing techniques described above are likely to be necessary, even if the chip includes one or more of the embedded memory testing techniques just described. The BIST and/or boundary scan circuitry may do no more than confirm that the embedded memory is bad. The failure analysis engineer must determine the specific cause of the failure, usually beginning by identifying the specific location in the memory array where the failure occurs--called bit mapping.

WEST

Generate Collection

L18: Entry 10 of 12 File: USPT Oct 11, 1994

DOCUMENT-IDENTIFIER: US 5355369 A
TITLE: High-speed integrated circuit testing with JTAG

DEPR:
Also included in the illustrative embodiment is a down-loadable digital processor architecture (see FIG. 2). The illustrative digital processor utilizes "harvard" architecture, which has separate address and data buses for "Instruction/Coefficient" and "Data". These buses communicate with the ALU (21), the arithmetic address unit AAU (23), and the controller (24). It also has dual port RAM (22) which communicates with both sets of buses. A program may be downloaded to the chip by having the digital processor core read an instruction as "Data" via one of its many data input mechanisms and writing it as "Data" to the dual port RAM. The instruction may then be executed from fetches over the "Instructions/Coefficient" buses from the dual port RAM. The scheme used in the illustrative processor uses a dual port memory associated with the digital processor core and having a size of typically at least 256 words. Note that unlike the BIST testing method, the memory requirement of the inventive testing technique does not necessarily add to chip area. This is because the memory may be re-used after testing for digital processor application programs and data. Although a dual-port memory is convenient for implementing the present invention, its use is not mandatory. For example, a Von Neumann architecture allows the use of a single-port memory. Note that the multiplexer 25, under control of signals CKTCK and SELCKI, provides a clock from any one of TCK (the JTAG test clock), CKI (the system clock used in normal chip operation), or JCKI (the scanned system clock).

L19: Entry 14 of 16 File: USPT Oct 11, 1994

DOCUMENT-IDENTIFIER: US 5355369 A
TITLE: High-speed integrated circuit testing with JTAG

DEPR:
Upon completion of the processing of the downloaded test program by the digital processor, the results are then uploaded to the TDR (50) from the data bus 54. This may be accomplished by directly writing the result to the TDR (a parallel bit transfer) by the digital processor, since the TDR is directly addressable therefrom. The result may then be serially scanned out via the JTAG output port TDO, according to the standard JTAG technique. In the illustrative arrangement of FIG. 4, the output passes through the bypass registers (408, 410, 412) of the chips (407, 409, 411) following the target chip. Note that the result of the test is typically several words, which require several such transfers. However, it is alternatively possible to compress the resulting words into fewer words, or even only one word, for transfer through the TDO port. Although an integrated circuit that implements the present invention may also implement all of the standard JTAG functions, that is not necessary in all cases. For example, the boundary-scan register may be omitted, while still advantageously implementing the present test using the TAP controller, instruction decoder, and TDI, TDO, TMS, and TCK pins on the integrated circuit. The prior-art use of user test registers (306) for implementing BIST may also be included in IC's that implement the present invention. Still other variations are possible, and included herein.

WEST

Generate Collection

L19: Entry 2 of 16 File: USPT May 30, 2000

DOCUMENT-IDENTIFIER: US 6070252 A
TITLE: Method and apparatus for interactive built-in-self-testing with user-programmable test patterns

BSPR:
Although the boundary-scan technique provides access to the input and output pins of an IC, the technique does not permit any access to the complex internal units of the chip. Accordingly, manufacturers have incorporated test equipment for executing a built-in self-test (BIST) directly into the loaded boards and the circuits. This built-in test equipment may be directly integrated into the hardware of the functional units to be tested, or encoded into microcode ROM. The BIST routine can be invoked by asserting a Self-Test pin on the processor or by using a JTAG

WEST

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L16: Entry 1 of 11 File: USPT Aug 22, 2000

DOCUMENT-IDENTIFIER: US 6108798 A
TITLE: Self programmed built in self test

DEPR:
Table 2 represents the steps in executing a test pattern known in the art as a MARCH pattern using the bit correspondence of Table 1. Self testing the prior art DRAM of FIG. 2 is initiated when XWE and XCAS occur before XRAS, an occurrence or condition referred to in the art as Write and CAS Before RAS (WCBR). A WCBR occurrence places the DRAM in test mode, activates the BIST enable signal and isolates CLKGEN 102, Address Buffer 104 and I/O circuit 106 from the chip internal operation. Instead of passing the DRAM control clocks, CLKGEN 102 generates an internal CLOCK for the BIST engine 200. Internal voltages and timings are set dependent upon values in the voltage table 216 and the timing table 218 before each microinstruction is executed.

DEPR:
First, System Clock Generator 4220 generates an internal clock that enables the BIST logic 4202. Internal voltages and timings are selected before execution of each initial microinstruction from the Voltage Table 4216 and Timing Table 4218.